P@RTAL
USPTO

Search: ⊙ The ACM Digital Library   ○ The Guide

| +mapping +digital +level | **SEARCH** |

▮ THE ACM DIGITAL LIBRARY ▮
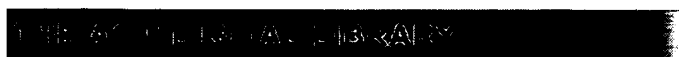
▮ Feedback Report a problem Satisfaction survey

Terms used **mapping** **digital** **level**   Found **25,129** of **160,172**

Sort results by	relevance ▾	● Save results to a Binder	Try an Advanced Search
Display results	expanded form ▾	② Search Tips ▢ Open results in a new window	Try this search in The ACM Guide

Results 1 - 20 of 200   Result page: **1** 2 3 4 5 6 7 8 9 10   next
Best 200 shown   Relevance scale ▢ ▢ ◪ ◼ ◼

1 Color gamut mapping and the printing of digital color images   ◼
Maureen C. Stone, William B. Cowan, John C. Beatty
October 1988 **ACM Transactions on Graphics (TOG)**, Volume 7 Issue 4

Full text available: 🔲 pdf(6.06 MB)   Additional Information: full citation, abstract, references, citings, index terms, review

Principles and techniques useful for calibrated color reproduction are defined. These results are derived from a project to take digital images designed on a variety of different color monitors and accurately reproduce them in a journal using digital offset printing. Most of the images printed were reproduced without access to the image as viewed in its original form; the color specification was derived entirely from calorimetric specification. The techniques described here are not specific ...

2 Digital sensor simulation: 1980-1985   ◼
Marshall B. Faintich
January 1980 **Proceedings of the 13th annual symposium on Simulation**

Full text available: 🔲 pdf(805.52 KB)   Additional Information: full citation, abstract, references, index terms

The Defense Mapping Agency is producing global digital data bases to support aircrew training simulators and other computer image generation systems. The evolution to digital sensor simulation is presented and current digital data bases are described. The refinement of actual sensors is changing the content required in these data bases, and the effect on digital sensor simulation in the 1980-1985 time period is discussed.

3 NSDL: Creating virtual collections in digital libraries: benefits and implementation issues   ◼
Gary Geisler, Sarah Giersch, David McArthur, Marty McClelland
July 2002 **Proceedings of the 2nd ACM/IEEE-CS joint conference on Digital libraries**

Full text available: 🔲 pdf(822.96 KB)   Additional Information: full citation, abstract, references, citings, index terms

Digital libraries have the potential to not only duplicate many of the services provided by traditional libraries but to extend them. Basic finding aids such as search and browse are common in most of today's digital libraries. But just as a traditional library provides more than a card catalog and browseable shelves of books, an effective digital library should offer a wider range of services. Using the traditional library concept of special collections as a model, in this paper we propose that ...

Keywords: collection, digital library, metadata, user services

4 Technology mapping and retargeting for field-programmable analog arrays

Sree Ganesan, Ranga Vemuri

January 2000 **Proceedings of the conference on Design, automation and test in Europe**

Full text available: pdf(137.04 KB)

Additional Information: full citation, references, citings, index terms

Publisher Site

5 Behavioral partitioning in the synthesis of mixed analog-digital systems

Sree Ganesan, Ranga Vemuri

June 2001 **Proceedings of the 38th conference on Design automation**

Full text available: pdf(152.55 KB)   Additional Information: full citation, abstract, references, index terms

Synthesis of mixed-signal designs from behavioral specifications must address analog-digital partitioning. In this paper, we investigate the issues in mixed-signal behavioral partitioning and design space exploration for signal-processing systems. We begin with the system behavior specified in an intermediate format called the Mixed Signal Flow Graph, based on the time-amplitude characterization of signals. We present techniques for analog-digital behavioral partitioning of the MSFG, and pe ...

6 Terrain database interoperability issues in training with distributed interactive simulation

Guy A. Schiavone, S. Sureshchandran, Kenneth C. Hardis

July 1997 **ACM Transactions on Modeling and Computer Simulation (TOMACS)**, Volume 7
Issue 3

Full text available: pdf(443.34 KB)   Additional Information: full citation, abstract, references, citings, index terms, review

In Distributed Interactive Simulation (DIS), each participating node is responsible for maintaining its own model of the synthetic environment. Problems may arise if significant inconsistencies are allowed to exist between these separate world views, resulting in unrealistic simulation results or negative training, and a corresponding degradation of interoperability in a DIS simulation exercise. In the DIS community, this is known as the simulator terrain database (TDB) correlation problem. ...

Keywords: distributed interactive simulation, terrain databases

7 A keystroke level analysis of a graphics application: manual map digitizing

Peter Haunold, Werner Kuhn

April 1994 **Proceedings of the SIGCHI conference on Human factors in computing systems: celebrating interdependence**

Full text available: pdf(772.23 KB)   Additional Information: full citation, references, citings, index terms

Keywords: Keystroke-Level Model, geographic information systems, graphics, interface design optimization, map digitizing

8 Concept mapping: an innovative approach to digital library design and evaluation

June P. Mead, Geri Gay

December 1995 **ACM SIGOIS Bulletin**, Volume 16 Issue 2

Full text available: pdf(580.83 KB)   Additional Information: full citation, abstract, citings, index terms

The Interactive Multimedia Group (IMG) at Cornell University has been designing and researching the impact of collaborative multimedia technologies on educational environments for over ten years. In one of our current projects, the Making of America, the IMG is focusing on the development of tools to support access to digital libraries. This effort is complemented by parallel research into the cognitive, behavioral, and social implications of using these systems. Additionally, the IMG is working ...

9 Design of a scalable parallel switch-level simulator for VLSI

R. B. Mueller-Thus, D. G. Saab, J. A. Abraham

November 1990 **Proceedings of the 1990 ACM/IEEE conference on Supercomputing**

Full text available: pdf(912.02 KB)   Additional Information: full citation, abstract, references

This paper deals with the problem of mapping a computation-intensive task of irregular structure onto a parallel framework. Our application is the switch-level logic simulation of digital circuits, a technique that is in wide use for the verification of VLSI designs. We focus on medium- grain multiprocessors (shared memory or message passing machines) and only consider *model parallel* computation, where the model of the design to be simulated is partitioned among processors. We address the ...

10 An hierarchical language for the structural description of digital systems

W. M. vanCleemput

January 1977 **Proceedings of the 14th conference on Design automation**

Full text available: pdf(500.70 KB)   Additional Information: full citation, abstract, references, citings, index terms

In this report a language (SDL) for describing structural properties of digital systems will be presented. SDL can be used at all levels of the design process i. e. from the system level down to the circuit level. The language is intended as a complement to existing computer hardware description languages, which emphasize behavioural description.The language was motivated partly by the nature of the design process.

11 Delay minimization and technology mapping of two-level structures and implementation using clock-delayed domino logic

Jovanka Ciric, Gin Yee, Carl Sechen

January 2000 **Proceedings of the conference on Design, automation and test in Europe**

Full text available: pdf(72.74 KB) Publisher Site   Additional Information: full citation, references, index terms

12 Using codesign techniques to support analog functionality

Francis G. Wolff, Michael J. Knieser, Dan J. Weyer, Chris A. Papachristou

March 1999 **Proceedings of the seventh international workshop on Hardware/software codesign**

Full text available: pdf(433.76 KB)   Additional Information: full citation, references, index terms

Keywords: analog, design methodologies, hardware/software codesign

13 Repartitioning and technology mapping of electronic hybrid systems

C. Grimm, K. Waldschmidt

February 1998 **Proceedings of the conference on Design, automation and test in Europe**

Full text available: pdf(239.80 KB)
Publisher Site

Additional Information: full citation, abstract, references, index terms

The systematic top-down design of mixed-signal systems requires an abstract specification of the intended functions. However, hybrid systems are systems whose parts are specified using different time models. Specifications of hybrid systems are not purely functional as they also contain structural information. The structural information is introduced by partitioning the specification into blocks with a homogeneous time model. This often leads to inefficient implementations. In order to overcome ...

Keywords: specification of hybrid systems, mixed-signal systems, top-down methodology, design automation, partitioning

14 Archiving, digital collections, and analysis: An evolutionary approach to digital recording and information about heritage sites

John Counsell
November 2001 **Proceedings of the 2001 conference on Virtual reality, archeology, and cultural heritage**

Full text available: pdf(3.32 MB)

Additional Information: full citation, abstract, references, citings, index terms

This paper considers 3 cases undertaken by a team at the University of the West of England (FBE/UWE) --- the Tower of London Computer Models and more recent linked European Historic Gardens on the Web. The team is continuing to investigate uses of spatial information systems to store, manage and visualise records of historic sites, enabling interactive off-site access to interpretative information. Existing records, often accrued in an ad-hoc manner, are mostly inadequate for such use and incomp ...

Keywords: GIS, VRML, augmented reality, real-time video, spatial information system

15 High-level library mapping for memories

Pradip K. Jha, Nikil D. Dutt
July 2000 **ACM Transactions on Design Automation of Electronic Systems (TODAES)**, Volume 5 Issue 3

Full text available: pdf(209.38 KB)

Additional Information: full citation, abstract, references, citings, index terms

We present high-level library mapping, a technique that synthesizes a source memory module from a library of target memory modules. In this paper, we define the problem of high-level library mapping for memories, identify and solve the three subproblems associated with this task, and finally combine these solutions into a suite of two memory mapping algorithms. Experimental results on a number of memory-intensive designs demonstrate that our memory mapping approach generates a wide variety ...

Keywords: high-level synthesis, memory libraries, technology-mapping

16 Compiler-directed page coloring for multiprocessors

Edouard Bugnion, Jennifer M. Anderson, Todd C. Mowry, Mendel Rosenblum, Monica S. Lam
September 1996 **Proceedings of the seventh international conference on Architectural support for programming languages and operating systems**, Volume 31 , 30 Issue 9 , 5

Full text available: pdf(1.37 MB)

Additional Information: full citation, abstract, references, citings, index terms

This paper presents a new technique, *compiler-directed page coloring,* that eliminates conflict misses in multiprocessor applications. It enables applications to make better use of the increased aggregate cache size available in a multiprocessor. This technique uses the compiler's knowledge of the access patterns of the parallelized applications to direct the operating system's virtual memory page mapping strategy. We demonstrate that this technique can lead to significant performance impr ...

17 Poster session: Making area-performance tradeoffs at the high level using the AccelFPGA compiler for FPGAs

P. Banerjee, V. Saxena, J. Uribe, M. Haldar, A. Nayak, V. Kim, D. Bagchi, S. Pal, N. Tripathi, R. Anderson

February 2003 **Proceedings of the 2003 ACM/SIGDA eleventh international symposium on Field programmable gate arrays**

Full text available: 📄 pdf(187.05 KB)   Additional Information: full citation, abstract

Applications such as digital cell phones, 3G wireless receivers, and voice over IP, require DSP functions that are typically mapped onto general purpose DSP processors. With the introduction of advanced FPGA architectures which provide built-in DSP support such as the Xilinx Virtex-II, and the Altera Stratix, a new hardware alternative is available for DSP designers. DSP design has traditionally been divided into algorithm development and hardware/software implementation. The majority of DSP alg ...

18 Texture mapping 3D models of real-world scenes

Frederick M. Weinhaus, Venkat Devarajan

December 1997 **ACM Computing Surveys (CSUR)**, Volume 29 Issue 4

Full text available: 📄 pdf(1.98 MB)   Additional Information: full citation, abstract, references, index terms, review

Texture mapping has become a popular tool in the computer graphics industry in the last few years because it is an easy way to achieve a high degree of realism in computer-generated imagery with very little effort. Over the last decade, texture-mapping techniques have advanced to the point where it is possible to generate real-time perspective simulations of real-world areas by texture mapping every object surface with texture from photographic images of these real-world areas. The techniqu ...

Keywords: anti-aliasing, height field, homogeneous coordinates, image perspective transformation, image warping, multiresolution data, perspective projection, polygons, ray tracing, real-time scene generation, rectification, registration, texture mapping, visual simulators, voxels

19 Digital libraries for spatial data: The ADEPT digital library architecture

Greg Janée, James Frew

July 2002 **Proceedings of the 2nd ACM/IEEE-CS joint conference on Digital libraries**

Full text available: 📄 pdf(263.61 KB)   Additional Information: full citation, abstract, references, citings, index terms

The Alexandria Digital Earth ProtoType (ADEPT) architecture is a framework for building distributed digital libraries of georeferenced information. An ADEPT system comprises one or more autonomous libraries, each of which provides a uniform interface to one or more collections, each of which manages metadata for one or more items. The primary standard on which the architecture is based is the ADEPT bucket framework, which defines uniform client-level metadata query services that are compatible w ...

Keywords: bucket framework, collection discovery, distribution, interoperability, metadata

20 Model checking of hierarchical state machines

Rajeev Alur, Mihalis Yannakakis
May 2001 **ACM Transactions on Programming Languages and Systems (TOPLAS),**
Volume 23 Issue 3

Full text available: pdf(453.28 KB)   Additional Information: full citation, abstract, references, index terms

Model checking is emerging as a practical tool for detecting logical errors in early stages of system design. We investigate the model checking of sequential hierarchical (nested) systems, i.e., finite-state machines whose states themselves can be other machines. This nesting ability is common in various software design methodologies, and is available in several commercial modeling tools. The straightforward way to analyze a hierarchical machine is to flatten it (thus incurring an exponential bl ...

Keywords: Hierarchical state machines, model checking, statecharts, temporal logic

Results 1 - 20 of 200   Result page: **1** 2 3 4 5 6 7 8 9 10   next

Useful downloads: Adobe Acrobat   QuickTime   Windows Media Player   Real Player

IEEE Xplore ® RELEASE 2.1

Welcome United States Patent and Trademark Office

⌐□ **Search Results**   BROWSE   SEARCH   IEEE XPLORE GUIDE

Results for "(mapping <in>metadata) <and> (digital <in>metadata) <and> (level<i..."   ☑ e-mail
Your search matched **587** of **1225093** documents.
A maximum of **100** results are displayed, **25** to a page, sorted by **Relevance** in **Descending** order.

» Search Options

View Session History

New Search

» Other Resources
(Available For Purchase)

Top Book Results

Integrated Circuit Manufacturability

by Gyvez, J. P. D.; Pradhan, D.;

Low-Power CMOS Design
by Chandrakasan, A.; Brodersen,
R. W.;

View All 2 Result(s)

» Key

IEEE JNL	IEEE Journal or Magazine
IEE JNL	IEE Journal or Magazine
IEEE CNF	IEEE Conference Proceeding
IEE CNF	IEE Conference Proceeding
IEEE STD	IEEE Standard

Modify Search

(mapping <in>metadata) <and> (digital <in>metadata) <and> (level<in>metadata [»]

☐ Check to search only within this results set

Display Format: ⦿ Citation   ○ Citation & Abstract

Select   Article Information   View: 1-25 | 26-5

☐ 1. **Hierarchical tolerance analysis using statistical behavioral models**
Koskinen, T.; Cheung, P.Y.K.;
Computer-Aided Design of Integrated Circuits and Systems, IEEE Transaction:
Volume 15, Issue 5, May 1996 Page(s):506 - 516
Digital Object Identifier 10.1109/43.506138

AbstractPlus | References | Full Text: PDF(976 KB)   IEEE JNL

☐ 2. **A study of farmland landscape pattern with TM and DEM. Case study in Y County, Yunnan Province, P.R.China**
Ning Wu; Chengqi Cheng; Shide Guo; Wenjie Fan; Xiru Xu; Yanglin Wang;
Geoscience and Remote Sensing Symposium, 2004. IGARSS '04. Proceeding International
Volume 5, 2004 Page(s):3420 - 3423 vol.5
Digital Object Identifier 10.1109/IGARSS.2004.1370440

AbstractPlus | Full Text: PDF(643 KB)   IEEE CNF

☐ 3. **Using lane tracker data to improve lane-level digital maps created with pr**
Wenbing Zhang; Taliwal, V.;
Intelligent Transportation Systems, 2003. Proceedings. 2003 IEEE
Volume 1, 2003 Page(s):585 - 589 vol.1
Digital Object Identifier 10.1109/ITSC.2003.1252020

AbstractPlus | Full Text: PDF(386 KB)   IEEE CNF

☐ 4. **Mapping physical defects to logic level for defect oriented testing**
Ubar, R.;
Signals, Circuits and Systems, 2003. SCS 2003. International Symposium on
Volume 2, 10-11 July 2003 Page(s):453 - 456 vol.2

AbstractPlus | Full Text: PDF(331 KB)   IEEE CNF

☐ 5. **Content layer progressive coding of digital maps**
Forchhammer, S.; Jensen, O.R.;
Data Compression Conference, 2000. Proceedings. DCC 2000
28-30 March 2000 Page(s):233 - 242
Digital Object Identifier 10.1109/DCC.2000.838163

AbstractPlus | Full Text: PDF(316 KB)   IEEE CNF

☐ 6. **Symbolic synthesis of analog-to-digital conversion architectures using d**

techniques
Weibiao Zhang; Huimin Xia; Al-Omari, R.; Hassoun, M.;
Electronics, Circuits and Systems, 1998 IEEE International Conference on
Volume 3, 7-10 Sept. 1998 Page(s):215 - 218 vol.3
Digital Object Identifier 10.1109/ICECS.1998.813970

AbstractPlus | Full Text: PDF(336 KB)   IEEE CNF

7. **Equalisation of analogue to digital converter nonlinearities**
Dent, A.C.; Smith, M.J.; Cowan, C.F.N.;
Circuits and Systems, 1988., IEEE International Symposium on
7-9 June 1988 Page(s):2201 - 2204 vol.3
Digital Object Identifier 10.1109/ISCAS.1988.15381

AbstractPlus | Full Text: PDF(252 KB)   IEEE CNF

8. **The European digital road map triggered by car information systems**
Bastiaansen, A.;
Intelligent Vehicles '94 Symposium, Proceedings of the
24-26 Oct. 1994 Page(s):582 - 583
Digital Object Identifier 10.1109/IVS.1994.639582

AbstractPlus | Full Text: PDF(168 KB)   IEEE CNF

9. **High-level software synthesis for the design of communication systems**
Ritz, S.; Pankert, M.; Zivojinovic, V.; Meyr, H.;
Selected Areas in Communications, IEEE Journal on
Volume 11, Issue 3, April 1993 Page(s):348 - 358
Digital Object Identifier 10.1109/49.219550

AbstractPlus | Full Text: PDF(1064 KB)   IEEE JNL

10. **Optimal PWM design for high power three-level inverter through compar**
Liu, H.L.; Cho, G.H.; Park, S.S.;
Power Electronics, IEEE Transactions on
Volume 10, Issue 1, Jan. 1995 Page(s):38 - 47
Digital Object Identifier 10.1109/63.368462

AbstractPlus | Full Text: PDF(760 KB)   IEEE JNL

11. **Contrast mapping and evaluation for electronic X-ray images on CRT dis**
Suzuki, J.; Furukawa, I.; Ono, S.; Kitamura, M.; Ando, Y.;
Medical Imaging, IEEE Transactions on
Volume 16, Issue 6, Dec. 1997 Page(s):772 - 784
Digital Object Identifier 10.1109/42.650874

AbstractPlus | References | Full Text: PDF(252 KB)   IEEE JNL

12. **Terrain intervisibility-believe it or not?**
Stiles, P.N.;
Aerospace and Electronic Systems Magazine, IEEE
Volume 16, Issue 8, Aug. 2001 Page(s):25 - 30
Digital Object Identifier 10.1109/62.942216

AbstractPlus | References | Full Text: PDF(704 KB)   IEEE JNL

13. **High-level synthesis of DSP datapaths by global optimisation of variable**
Duncan, A.A.; Hendry, D.C.;
Computers and Digital Techniques, IEE Proceedings-
Volume 142, Issue 3, May 1995 Page(s):215 - 224

AbstractPlus | Full Text: PDF(788 KB)   IEE JNL

14. **Overview of the FREEDOM compiler for mapping DSP software to FPGAs**
Zaretsky, D.; Mittal, M.; Xiaoyong Tang; Banerjee, P.;
Field-Programmable Custom Computing Machines, 2004. FCCM 2004. 12th A

Symposium on
20-23 April 2004 Page(s):37 - 46
Digital Object Identifier 10.1109/FCCM.2004.44

AbstractPlus | Full Text: PDF(400 KB)   IEEE CNF

15. **Constructing 3D city models by merging ground-based and airborne viev**
Frueh, C.; Zakhor, A.;
Computer Vision and Pattern Recognition, 2003. Proceedings. 2003 IEEE Cor
Conference on
Volume 2, 18-20 June 2003 Page(s):II - 562-9 vol.2
Digital Object Identifier 10.1109/CVPR.2003.1211517

AbstractPlus | Full Text: PDF(801 KB)   IEEE CNF

16. **Mapping total environmental sound exposure of bottlenose dolphins, tur.
in the Wilmington, north Carolina intracoastal waterway**
Haviland, G.M.; Sayigh, L.S.; Frankel, A.S.; Powell, C.M.; Bocconcellil, A.; Her
OCEANS, 2001. MTS/IEEE Conference and Exhibition
Volume 3, 5-8 Nov. 2001 Page(s):1392 - 1394 vol.3
Digital Object Identifier 10.1109/OCEANS.2001.968037

AbstractPlus | Full Text: PDF(248 KB)   IEEE CNF

17. **Terrain intervisibility-believe it or not?**
Stiles, P.N.;
Digital Avionics Systems Conferences, 2000. Proceedings. DASC. The 19th
Volume 2, 7-13 Oct. 2000 Page(s):5A2/1 - 5A2/7 vol.2
Digital Object Identifier 10.1109/DASC.2000.884869

AbstractPlus | Full Text: PDF(600 KB)   IEEE CNF

18. **Citation retrieval in digital libraries**
Chen Ding; Chi-Hung Chi; Jing Deng; Chun-Lei Dong;
Systems, Man, and Cybernetics, 1999. IEEE SMC '99 Conference Proceeding
International Conference on
Volume 2, 12-15 Oct. 1999 Page(s):105 - 109 vol.2
Digital Object Identifier 10.1109/ICSMC.1999.825216

AbstractPlus | Full Text: PDF(408 KB)   IEEE CNF

19. **Biologically-inspired digital circuit for a self-organising neural network**
Perez, M.A.J.; Luque, W.M.; Damiani, F.;
Devices, Circuits and Systems, 1998. Proceedings of the 1998 Second IEEE I
Caracas Conference on
2-4 March 1998 Page(s):172 - 177
Digital Object Identifier 10.1109/ICCDCS.1998.705827

AbstractPlus | Full Text: PDF(512 KB)   IEEE CNF

20. **Design methodology for digital signal processing**
Fettweis, G.;
Application-Specific Systems, Architectures and Processors, 1997. Proceedinç
International Conference on
14-16 July 1997 Page(s):468 - 477
Digital Object Identifier 10.1109/ASAP.1997.606852

AbstractPlus | Full Text: PDF(552 KB)   IEEE CNF

21. **Algorithm-architecture mapping for custom DSP chips**
Loeffler, C.; Ligtenberg, A.; Moschytz, G.S.;
Circuits and Systems, 1988., IEEE International Symposium on
7-9 June 1988 Page(s):1953 - 1956 vol.2
Digital Object Identifier 10.1109/ISCAS.1988.15321

AbstractPlus | Full Text: PDF(272 KB)   IEEE CNF

☐ **22. VLSI design of inner-product computers using distributed arithmetic**
Burleson, W.P.; Scharf, L.L.;
Circuits and Systems, 1989., IEEE International Symposium on
8-11 May 1989 Page(s):158 - 161 vol.1
Digital Object Identifier 10.1109/ISCAS.1989.100316

AbstractPlus | Full Text: PDF(328 KB)   IEEE CNF

☐ **23. Design of a scalable parallel switch-level simulator for VLSI**
Mueller-Thuns, R.B.; Saab, D.G.; Abraham, J.A.;
Supercomputing '90. Proceedings of
12-16 Nov. 1990 Page(s):615 - 624
Digital Object Identifier 10.1109/SUPERC.1990.130077

AbstractPlus | Full Text: PDF(624 KB)   IEEE CNF

☐ **24. Matrix computations in arrays of DSPs**
Moreno, J.; Medina, M.;
Application Specific Array Processors, 1992. Proceedings of the International (
4-7 Aug. 1992 Page(s):496 - 510
Digital Object Identifier 10.1109/ASAP.1992.218549

AbstractPlus | Full Text: PDF(608 KB)   IEEE CNF

☐ **25. New mapboard concepts for electric operations**
Blaeser, P.;
Rural Electric Power Conference, 1994. Papers Presented at the 38th Annual
24-26 April 1994 Page(s):D3/1 - D3/8
Digital Object Identifier 10.1109/REPCON.1994.326245

AbstractPlus | Full Text: PDF(2684 KB)   IEEE CNF

View: **1-25** | 26-5

Help   Contact Us   Privacy & :

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	1	map$ centroid serie Ievel	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2005/08/19 12:45
L2	1	map$ centroid Ievel	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2005/08/19 12:45
L3	2089	mapping centroid level	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2005/08/19 12:45
L4	1471	mapping centroid level series	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2005/08/19 12:45
L5	0	mapping centroid level series	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	WITH	ON	2005/08/19 12:45
L6	2	mapping centroid level series	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	SAME	ON	2005/08/19 12:46
L7	1995	(341/144,145,150,153154,148,133).CCLS.	USPAT	OR	OFF	2005/08/19 12:46
L8	0	mapping centroid level series and L7	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	SAME	ON	2005/08/19 12:46
L9	0	mapping centroid level series and L7	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	SAME	ON	2005/08/19 12:46

L10	0	mapping centroid level and L7	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	SAME	ON	2005/08/19 12:46
L11	20	mapping level and L7	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	SAME	ON	2005/08/19 12:46
L12	11	mapping digital level and L7	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	SAME	ON	2005/08/19 12:46
S1	1995	(341/144,145,150,153154,148,133). CCLS.	USPAT	OR	OFF	2005/08/19 12:44